CLAIMS

1. A method for forming a thin-film transistor (TFT) on a flexible substrate, the method comprising:

supplying a metal foil substrate with a surface;

depositing amorphous silicon;

annealing the amorphous silicon to form polycrystalline silicon; and,

thermally growing a gate insulation film overlying the polycrystalline film.

2. The method of claim 1 wherein annealing the amorphous silicon to form polycrystalline silicon includes annealing at a temperature greater than 700 degrees C.

3. The method of claim 2 wherein annealing the amorphous silicon to form polycrystalline silicon includes using a solid-phase crystallization (SPC) annealing process.

4. The method of claim 1 wherein annealing the amorphous silicon to form polycrystalline silicon includes using a Laser-Induced Lateral Growth (LILaC) annealing process.

5. The method of claim 1 further comprising:

planarizing the metal foil substrate surface;

depositing an electrical isolation layer overlying the planarized metal foil substrate surface; and,

wherein depositing amorphous silicon includes depositing amorphous film overlying the electrical insulation layer.

6. The method of claim 5 further comprising:

patterning the silicon to form silicon islands; and,

wherein thermally growing a gate insulation film includes thermally growing a gate insulation layer overlying polycrystalline islands.

7. The method of claim 6 further comprising:

forming transistor gate, source, and drain regions.

8. The method of claim 1 wherein supplying a metal foil substrate with a surface includes supplying a metal foil material selected from the group including titanium (Ti), Inconel alloy, stainless steel, and Kovar.

9. The method of claim 8 wherein supplying a metal foil substrate with a surface includes supplying a metal foil having a thickness in the range of 10 to 500 microns.

10. The method of claim 9 wherein supplying a metal foil substrate with a surface includes supplying a metal foil having a thickness in the range of 50 to 250 microns.

11. The method of claim 10 wherein supplying a metal foil substrate with a surface includes supplying a metal foil having a thickness in the range of 100 to 200 microns.

12. The method of claim 5 wherein planarizing the metal foil substrate surface includes chemical-mechanical polishing (CMP) the metal foil substrate surface.

13. The method of claim 12 wherein chemical-mechanically polishing the metal foil substrate surface includes polishing to an average surface roughness of less than approximately 200 nanometers (nm).

14. The method of claim 5 wherein planarizing the metal foil substrate surface includes spin-coating a dielectric material overlying the metal foil substrate surface.

15. The method of claim 14 wherein spin-coating a dielectric material overlying the metal foil substrate surface includes forming a dielectric layer having a thickness in the range of 200 to 500 nm.

16. The method of claim 14 wherein spin-coating a dielectric material overlying the metal foil substrate surface includes forming a dielectric layer from a spin-on-glass (SOG) material.

17. The method of claim 5 wherein depositing an electrical isolation layer overlying the planarized metal foil substrate surface includes depositing an electrical isolation layer from a material selected from the group including SiO2, SiNx, and SiON.

18. The method of claim 17 wherein depositing an electrical isolation layer overlying the planarized metal foil substrate surface includes depositing a layer having a thickness in the range of 0.5 to 2 microns.

19. The method of claim 18 wherein depositing an electrical isolation layer overlying the planarized metal foil substrate surface includes depositing a layer having a thickness in the range of 0.5 to 1.5 microns.

20. The method of claim 19 wherein depositing an electrical isolation layer overlying the planarized metal foil substrate surface includes depositing a layer having a thickness in the range of 0.5 to 1 microns.

21. The method of claim 1 further comprising:

following the deposition of the amorphous silicon, p-doping the amorphous silicon to adjust the threshold voltage.

22. The method of claim 3 wherein using a SPC annealing process includes using a process selected from the group including furnace and rapid-thermal annealing (RTA).

23. The method of claim 22 wherein annealing the amorphous silicon at a temperature greater than 700 degrees C includes annealing at a temperature in the range of 700 to 1000 degrees C for a period of time in the range of 2 seconds to 30 minutes.

24. The method of claim 23 wherein annealing the amorphous silicon at a temperature greater than 700 degrees C includes annealing at a temperature in the range of 750 to 950 degrees C for a period of time in the range of 2 seconds to 30 minutes.

25. The method of claim 1 wherein thermally growing a gate insulation film includes:

forming a first film polycrystalline silicon layer; and,

thermally oxidizing the first film layer.

26. The method of claim 25 wherein thermally oxidizing the first film layer includes annealing at temperature in the range of 900 to 1150 degrees C for a period of time in the range of 2 to 60 minutes.

27. The method of claim 26 wherein forming a first film polycrystalline silicon layer includes forming a first film layer having a thickness in the range of 10 to 100 nanometers (nm).

28. The method of claim 25 wherein thermally growing a gate insulation film further includes plasma depositing a second layer of oxide overlying the first film.

29. The method of claim 28 wherein forming a first film layer includes depositing a first film layer having a thickness in the range of 10 to 50 nm.

30. The method of claim 29 wherein depositing a first film layer includes depositing a layer having a thickness in the range of 20 to 30 nm.

31. The method of claim 29 wherein plasma depositing a second layer of oxide overlying the first film includes depositing a layer having a thickness in the range of 40 to 100 nm.

32. The method of claim 31 wherein plasma depositing a second layer of oxide overlying the first film includes depositing a layer having a thickness in the range of 50 to 70 nm.

33. The method of claim 28 wherein plasma depositing a second layer of oxide overlying the first film includes depositing a TEOS-SiO2 material.

34. The method of claim 6 wherein patterning the silicon to form silicon islands includes patterning polycrystalline islands following the annealing of the amorphous silicon.

35. The method of claim 6 wherein patterning the silicon to form silicon islands includes patterning amorphous silicon islands prior to annealing of the amorphous silicon.

36. The method of claim 1 wherein depositing amorphous silicon includes depositing amorphous silicon having a thickness in the range of 25 to 150 nm.

37. The method of claim 36 wherein depositing amorphous silicon includes depositing amorphous silicon having a thickness in the range of 25 to 100 nm.

38. The method of claim 37 wherein depositing amorphous silicon includes depositing amorphous silicon having a thickness in the range of 35 to 60 nm.

39. A method for forming a thin-film transistor (TFT) on a flexible substrate, the method comprising:

supplying a metal foil substrate with a surface;

planarizing the metal foil substrate surface;

depositing an electrical isolation layer overlying the planarized metal foil substrate surface;

depositing amorphous silicon overlying the electrical isolation layer;

annealing the amorphous silicon at a temperature greater than 700 degrees C to form polycrystalline silicon; and,

thermally growing a gate insulation film.

40. A thin-film transistor (TFT) on a flexible substrate comprising:

a metal foil substrate with a surface;

an electrical isolation layer overlying the metal foil substrate surface;

drain, source, and channel regions formed from polycrystalline silicon overlying the electrical isolation layer;

a gate insulation oxide film overlying the polycrystalline silicon having an index of refraction in the range of 1.4 to 1.6; and,

a gate overlying the gate insulation oxide layer.

41. The TFT of claim 40 wherein the metal foil substrate has a thickness in the range of 10 to 500 microns.

42. The TFT of claim 41 wherein the metal foil substrate has a thickness in the range of 50 to 250 microns.

43. The TFT of claim 42 wherein the metal foil substrate has a thickness in the range of 100 to 200 microns.

44. The TFT of claim 40 wherein the metal foil substrate surface has an average surface roughness of less than approximately 200 nanometers (nm).

45. The TFT of claim 40 further comprising:

a spin-coat dielectric material overlying the metal foil substrate having a thickness in the range of 200 to 500 nm.

46. The TFT of claim 45 wherein the spin-coat dielectric material is a spin-on-glass (SOG) material.

47. The TFT of claim 40 wherein the electrical isolation layer is a material selected from the group including SiO2, SiNx, and SiON.

48. The TFT of claim 47 wherein the electrical isolation layer has a thickness in the range of 0.5 to 2 microns.

49. The TFT of claim 48 wherein the electrical isolation layer has a thickness in the range of 0.5 to 1.5 microns.

50. The TFT of claim 49 wherein the electrical isolation layer has a thickness in the range of 0.5 to 1 microns.

51. The TFT of claim 40 wherein the polycrystalline silicon has a thickness in the range of 25 to 150 nm.

52. The TFT of claim 51 wherein the polycrystalline silicon has a thickness in the range of 25 to 100 nm.

53. The TFT of claim 52 wherein the polycrystalline silicon has a thickness in the range of 35 to 60 nm.

54. The TFT of claim 40 wherein the gate insulation oxide film has a thickness in the range of 10 to 100 nm.

55. The TFT of claim 54 wherein the gate insulation oxide film includes:

a first oxide film layer having an index of refraction in the range of 1.4 to 1.6; and,

a second oxide film layer overlying the first oxide layer having an index of refraction in the range of 1.4 to 2.0.

56. The TFT of claim 55 wherein the first oxide film layer has a thickness in the range of 20 to 30 nm.

57. The TFT of claim 55 wherein the second oxide film layer has a thickness in the range of 40 to 100 nm.

58. The TFT of claim 57 wherein the second oxide film layer has a thickness in the range of 50 to 70 nm.

59. The TFT of claim 55 wherein the second oxide film layer is a SiO2 material.

60. The TFT of claim 55 wherein the first oxide film layer is a SiO2 material.

61. The TFT of claim 40 wherein the metal foil substrate is a material selected from the group including titanium (Ti), Inconel alloy, stainless steel, and Kovar.